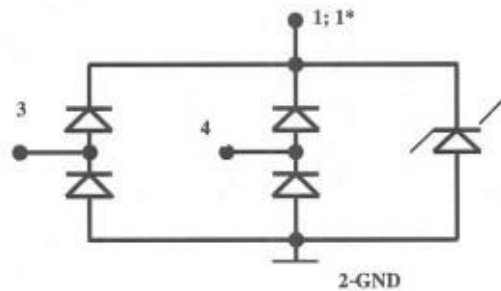
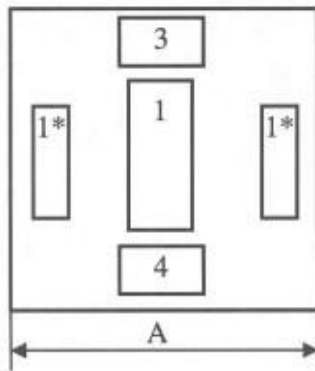



Chip Low Capacitance 2-line ESD protection.


Schematic and pinning diagram.

- Mechanical date: $A_x=A_y=1450\mu\text{m}$.
 Pad Size: 1 – $A_x=300\mu\text{m}$, $A_y=620\mu\text{m}$;
 1* - $A_x=165\mu\text{m}$, $A_y=540\mu\text{m}$; 3, 4 – $A_x=395\mu\text{m}$, $A_y=230\mu\text{m}$.
 Die thickness – $138\pm 12\mu\text{m}$
 Scribe Line Width – $60\mu\text{m}$.
 Pin 1, 1*, 3, 4 –Al metallization for wire bond .
 Thickness Al – $4,0\pm 0,4\mu\text{m}$.
 Pin 2 – Back side. Metallization Ti-Ni-Ag for soldering.

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Peak Pulse Power	P_{pp}	$t_p=2/10\mu\text{S}$	2500*	W
Peak Pulse Current	I_{pp}	$t_p=2/10\mu\text{S}$	120*	A
Peak Pulse Current	I_{pp}	$t_p=8/20\mu\text{S}$	95*	A
Electrostatic Discharge	V_{ESD}	IEC 61000-4-2, level 4. Contact and Air.	$\pm 30,0$	kV
Max.junction temperature	T_j		+125	°C

Characteristics . $T_j=25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_R	Reverse leakage current. Pins 3, 4 to ground	$V=+5,0\text{ V}$, $T=25^\circ\text{C}$.	-	-	0,9	μA
I_R	Reverse leakage current. Pins 3, 4 to pin 1.	$V= -5,0\text{ V}$, $T=25^\circ\text{C}$.	-	-	0,9	μA
V_{BR}	Reverse breakdown voltage. Pin 3,4 to ground.	$I_R=1\text{mA}$	6,1	-	-	V
V_F	Forward voltage . Pin 3, 4 to pin 1.	$I_F=95\text{A}$, $t_p=8/20\mu\text{S}$.	-	4,5*	-	V
V_F	Forward voltage . Pin 2 to pin 3, 4.	$I_F=95\text{A}$, $t_p=8/20\mu\text{S}$.	-	4,5*	-	V
$C_{I/O}$	Pin capacitance to ground. Pins 3, 4 to 2.	$V_R=0$; $f = 1\text{ MHz}$.	-	-	25	pF
$C_{I/O-I/O}$	Capacitance pin3 to pin4.	$V_R=0$; $f = 1\text{ MHz}$.	-	-	12	pF