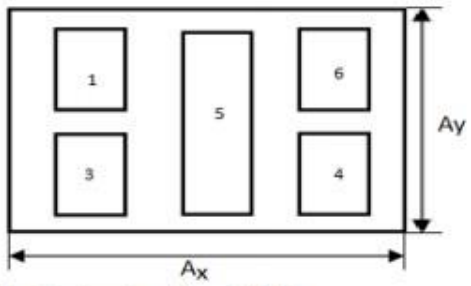
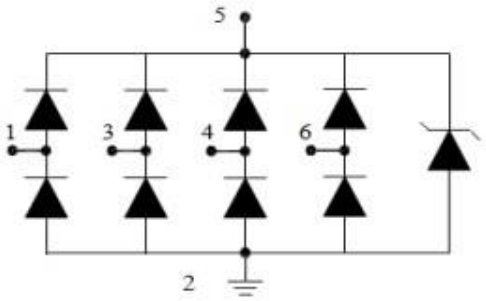
KSR-XXV4M6

Chip Low Capacitans TVS diode array.



Pin 2 – back side – GND



Schematic and pinning diagram

Mechanical data: A_x= 1000um, A_y=600um
Pad Size for Pin 1, 3, 4, 6 - 85 *95 um.
Pad Size for Pin 5 -270*105 um.
Chip thickness: 138+/-12um.
Scribe Line width - 60um.
Top Metal: Al - for wire bonding.
Back side - Anode: Ti-Ni-Ag for soldering
Probing:sampling testing: no bad dice inking guaranteed good dice quantity≥93%

Limiting values

Parameter	Symbol	Conditions	Value	Unit
Peak Pulse Power	P_{pp}	tp=8/20us	-	W
Peak Pulse Current	Ipp	tp=8/20us; Any I/O to Pin5; Pin2 to Any I/O.	25*	A
Electrostatic Discharge	VESD	IEC 61000-4-2. Any I/O to Pin5; Pin2 to Any I/O	+/-30 (Contact); +/-30 (Air).	kV
Max.junction temperature	Tj	-	+125	ºC

Characteristics (Ta=25ºC)

SYMBOL	PARAMETE	CONDITIONS	MIN.	TYP	MAX.	UNIT
VRWM	Reverse Stand-off voltage	-	-	-	3.3	V
VBR	Breakdown voltage	IR=1mA. Pin 5 to Pin 2.	5,0	-	-	V
IR	Reverse leakage current	V=+3,3V. Any I/O to Pin2. V=-3,3V. Any I/O to Pin 5.	-	-	0,3	uA
VF	Forward Voltage	IF=15mA. Pin 2 to Any I/O & Ani I/O to Pin5.	-	-	1,0	V
VCL	Forward Voltage	Ipp=1.0A, tp=8/20us Ipp=10.0A, tp=8/20us Ipp=25.0A, tp=8/20us;Any I/O to Pin 5.	- - -	- - -	1,0* 3,7* 8,2*	V
CJ	Capacitance. Any I/O pin to Ground	VR=0 V, f =1MHz	-		5,0	pF
CJ	Capacitance. Any I/O pin to I/O	VR=0 V, f =1MHz	-	-	2,5	pF

*- For Device testing