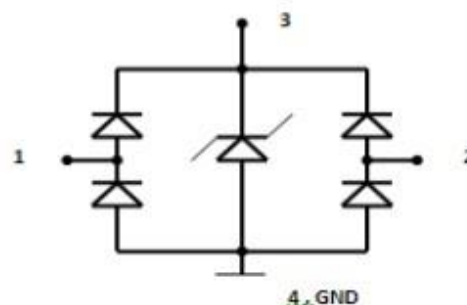
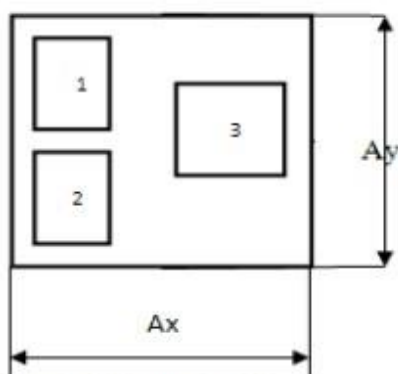



**EDS Protect for two unidirectional high-speed I/O channels**

**Schematic and pinning diagram**
**Mechanical data:**  $A_x=380\mu\text{m}$ ,  $A_y=420\mu\text{m}$ ,

 Pad size for Pin 1, 2 –  $80*90\mu\text{m}$ 

 Pad size for Pin 3 –  $140*100\mu\text{m}$ 

Pin 4 – back side – GND

**Chip thickness:** a)  $138\pm 12\mu\text{m}$ , b)  $470\pm 20\mu\text{m}$ 
**Scribe Line width** -  $40\mu\text{m}$ 
**Top Metal:** Al - for wire bonding

**Backside:** a) Ti-Ni-Ag for soldering, b) without metallization

**Probing:** 1) sampling testing – no bad dice inking, guaranteed good dice quantity  $\geq 93\%$ 

2) 100% testing (if agreed with customer) – wafer mapping data

**Limiting values**

Parameter	Symbol	Conditions	Value	Unit
Reverse Stand-Off Voltage	$V_{RWM}$	-	5	V
Peak pulse power - any I/O pin to Ground	$P_{PP}$	$t_p= 8/20 \mu\text{S}$	100**	W
Peak pulse current - any I/O pin to Ground	$I_{PP}$	$t_p= 8/20 \mu\text{S}$	4.0**	A
Electrostatic Discharge	$V_{ESD}$	IEC 61000-4-2, level 4	>15 (air); >8 (contact)	kV
Max.junction temperature	$T_j$	-	+125*	°C

**Characteristics ( $T_a=25^\circ\text{C}$ )**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Breakdown Voltage	$V_{BR}$	$I_R=1\text{mA}$ , Pin3 to Pin4	6.1	7.0	8.5	V
Reverse leakage current	$I_R$	$V=5\text{V}$ , Pin1,2,3 to Pin4 Pin3 to Pin1,2	-	-	0.9	$\mu\text{A}$
Forward voltage	$V_F$	$I_F=15\text{mA}$	-	-	1.15	V
Clamping Voltage – any I/O pin to Ground	$V_{CL}$	$I_{PP}=1\text{A}$ , $t_p=8/20\mu\text{S}$ ; $I_{PP}=4\text{A}$ , $t_p=8/20\mu\text{S}$	-	-	15** 25**	V
Capacitance – any I/O pin to Ground	$C_j$	$V_R=0\text{V}$ ; $f=1\text{MHz}$	-	-	0,8	pF
Capacitance – between I/O pins	$C_j$	$V_R=0\text{V}$ ; $f=1\text{MHz}$	-	-	0,4	pF

 \* -  $T_j=T_a+R_{th}(j-a)(P_f+P_r)$ , where  $R_{th}(j-a)$  – thermal resistance,  $P_f$  – forward power dissipation,

 $P_r$  – revers power dissipation

\*\* - For Device testing